

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200300253-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Philip J. Kuekes et al.

Confirmation No.:

Application No.: 10/659,892

Examiner:

Filing Date: Sept. 10, 2003

Group Art Unit:

Title: Defect-Tolerant and Fault-Tolerant Circuit Interconnections

Mail Stop PGPUB Drawings
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

DRAWING TRANSMITTAL LETTER

COPY

Sir:

Enclosed herewith please find:

- () _____ sheets of redlined drawing(s) which indicate proposed changes to the drawing(s). Upon approval of these proposed changes, formal drawing(s) will be submitted.
- () _____ sheets of corrected formal drawing(s), as required by the Notice of Patent Drawings Objection (PTO-948) which accompanied the Office Action dated _____.
- () _____ sheets of corrected formal drawing(s), as required by the Notice of Patent Drawings Objection (PTO-948) and approved in the Notice of Allowability dated _____.
- (X) 45 sheets of formal drawing(s). Please substitute these formal drawing(s) for the informal drawing(s) originally filed.
- () _____

Examiner's approval of the entry of these drawings is respectfully requested. No new matter has been added.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

Date of Deposit: **Dec. 11, 2003**

Typed Name: **Joanne Bourguignon**

Signature: 

Rev 85/03 (Dwgtrans)

Respectfully submitted,

Philip J. Kuekes et al.

By 

Robert W. Bergstrom

Attorney/Agent for Applicant(s)
Reg. No. **39,906**

Date: **Dec. 11, 2003**

Telephone No.: **(206) 621-1933**



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SENT: Dec. 11, 2003
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Formal Drawings

Kindly acknowledge receipt of the below-listed documents by placing
your receiving stamp hereon and mailing:

Drawing Transmittal; Forty-five sheets of drawings (Figs.1-29B); USAN 10/659,892; in
re:Philip J. Kuekes et al., for, DEFECT-TOLERANT AND FAULT-TOLERANT CIRCUIT
INTERCONNECTIONS.

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